Description

PJ53 Series are the high input very low I_Q and 300mA maximum output current LDO with enable function that operates from 1.8V~12V, is designed specifically for portable battery-powered applications which require ultra-low quiescent current. The very-low consumption of type 2.8uA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications.

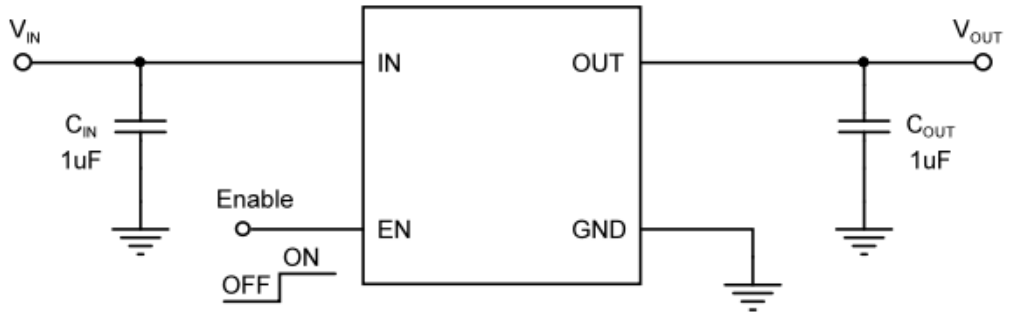
Features

- Wide Input Voltage Range: 3V~ 40V
- Maximum Output Current: 300mA
- Standard Fixed Output Voltage Options: 3.6V,5V,6V,7V,8V,12V,etc
- Low Quiescent Current: 2.8μA(Typ.)
- PSRR=50dB@1KHz
- Low Dropout : 1000mV @ 300mA(V_{OUT}=3.0V)
- Low Output Voltage Accuracy: ±1.5%(T_A=25℃)
- Excellent Load/Line Transient Response
- Available Packages: SOT-89, SOT-89-5, SOT-23-3, SOT-23-5, DFN1x1-4L,TO-252 and DFN2x2C-6L

Applications

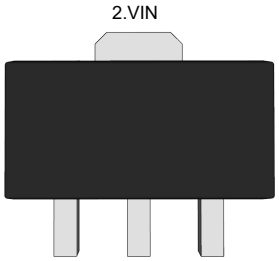
- Battery-Powered Equipment
- Smoke Detectors and Sensors
- Micro Controller Applications

Typical Application Circuit



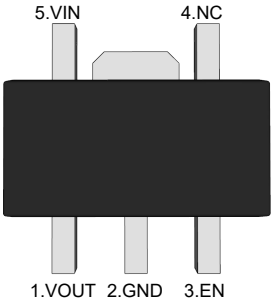
Pin Distribution

SOT-89



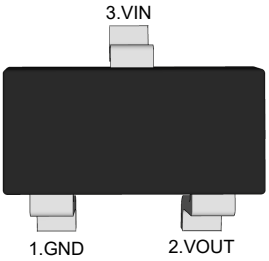
(Top View)

SOT-89-5



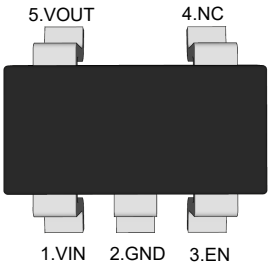
(Top View)

SOT-23-3



(Top View)

SOT-23-5

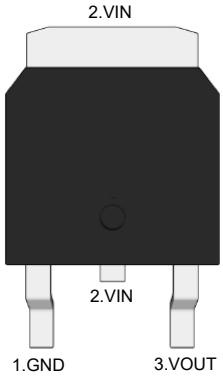


(Top View)

DFN1x1-4L

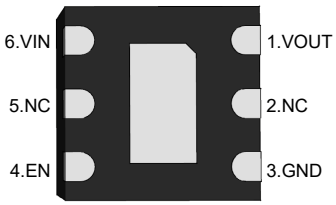
(Bottom View)

TO-252



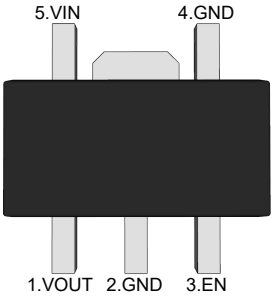
(Top View)

DFN2x2C-6L



Bottom View

SOT-89-5



(Top View)

PJ53-A Series

Functional Pin Description

Pin Name	Pin Function
VIN	Power Input Voltage
GND	Ground
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
VOUT	Output Voltage

Ordering Information

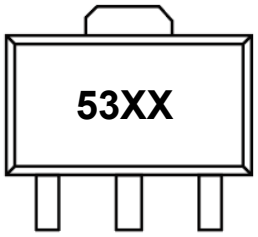
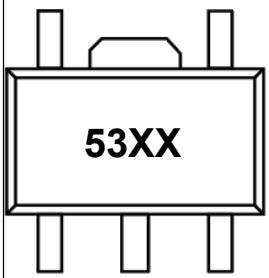
PJ53 □□□□□

Pin arrangement version number
□(Blank): Normal pin arrangement version
-A: A version pin arrangement

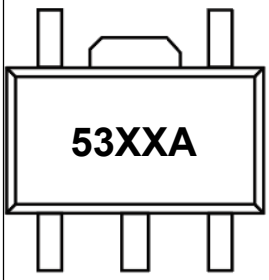
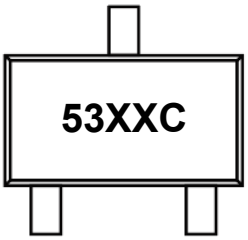
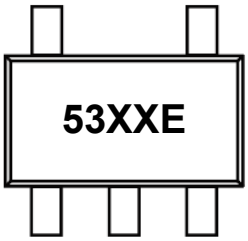
Package Type
SQ : SOT-89 SR : SOT-89-5
SC : SOT-23-3 SE : SOT-23-5
DE : DFN1x1-4L TE : TO-252 DFC : DFN2x2C-6L

Output Voltage
36 : 3.6V 50 : 5V 60 : 6V 70 : 7V
80: 8V 120: 12V

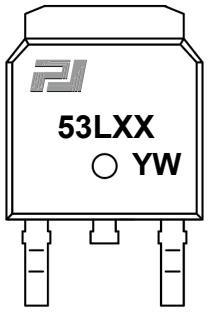
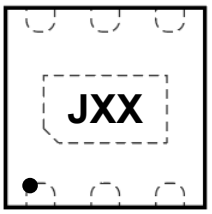
Output current tap
L : 300mA

Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan Note1	MSL Level	Marking Code
PJ53L36SQ	SOT-89	7/13	1000/3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50SQ						
PJ53L60SQ						
PJ53L70SQ						
PJ53L80SQ						
PJ53L120SQ						
PJ53L36SR	SOT-89-5	7/13	1000/3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50SR						
PJ53L60SR						
PJ53L70SR						
PJ53L80SR						
PJ53L120SR						

Ordering Information

Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan Note1	MSL Level	Marking Code
PJ53L36SR-A	SOT-89-5	7/13	1000/3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50SR-A						
PJ53L60SR-A						
PJ53L70SR-A						
PJ53L80SR-A						
PJ53L120SR-A						
PJ53L36SC	SOT-23-3	7	3000	RoHS & Green	MSL3	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50SC						
PJ53L60SC						
PJ53L70SC						
PJ53L80SC						
PJ53L120SC						
PJ53L36SE	SOT-23-5	7	3000	RoHS & Green	MSL3	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50SE						
PJ53L60SE						
PJ53L70SE						
PJ53L80SE						
PJ53L120SE						

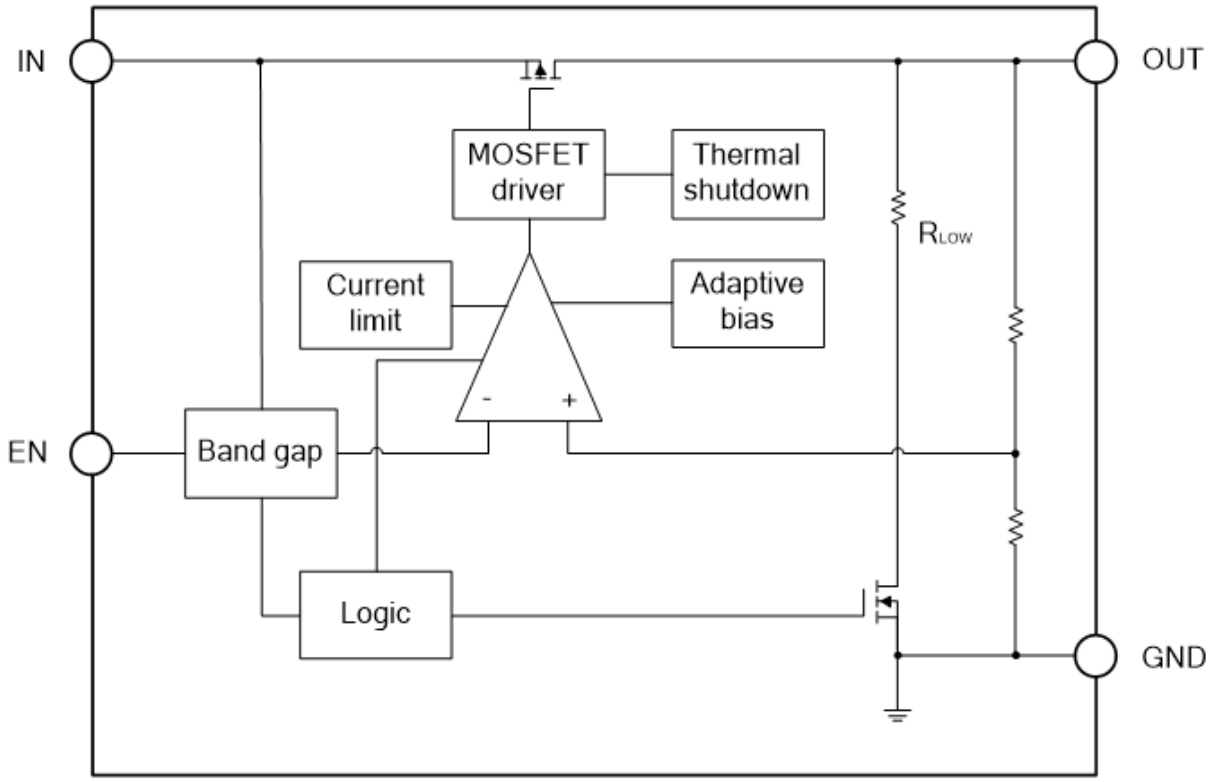
Ordering Information

Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan Note1	MSL Level	Marking Code
PJ53L36DE	DFN1x1-4L	7	10000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50DE						
PJ53L60DE						
PJ53L70DE						
PJ53L80DE						
PJ53L120DE						
PJ53L36TE	TO-252	13	2500	RoHS & Green	MSL3	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50TE						
PJ53L60TE						
PJ53L70TE						
PJ53L80TE						
PJ53L120TE						
PJ53L36DFC	DFN2x2C-6L	7	3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 36:3.6V, 120:12V
PJ53L50DFC						
PJ53L60DFC						
PJ53L70DFC						
PJ53L80DFC						
PJ53L120DFC						

Note:

1. RoHS：PJ defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials.
   Green：PJ defines "Green" to mean Halogen-Free and Antimony-Free.

Function Block Diagram



Absolute Maximum Ratings Note2

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
VIN to GND Voltage Note3		-0.3 ~ +43	V
VOUT to GND Voltage		0.8 ~ +15	V
EN to GND Voltage		-0.3 ~ +50	V
Power Dissipation Note4	SOT-89	920	mW
	SOT-89-5	920	mW
	SOT-23-3	500	mW
	SOT-23-5	500	mW
	DFN1x1-4L	500	mW
	TO-252	2500	mW
	DFN2x2C-6L	1700	mW
Thermal Resistance,Junction-to-Ambient	SOT-89	135	°C/W
	SOT-89-5	135	°C/W
	SOT-23-3	250	°C/W
	SOT-23-5	250	°C/W
	DFN1x1-4L	250	°C/W
	TO-252	50	°C/W
	DFN2x2C-6L	73	°C/W
Maximum Junction temperature		150	°C
Storage temperature range		-55 ~ +150	°C
ESD(HBM) Note5		2000	V
ESD(CDM) Note5		1500	V
Latch Up Current Maximum Rating Note5		200	mA

Note: 2. Exceed these limits to damage to the device, exposure to absolute maximum rating conditions may affect the reliability of the chip.
3. Refer to electrical eharacteristics and application information for safe operating area.
4. PCB board dimension : 40mm x 40mm (2layer) copper :1OZ
5. This device series incorporates ESD protection and is tested by the following methods:
ESD HBM tested per EIA/JESD22-A114;
ESD CDM tested per JESD22-C101;
Latch up tested per JEDEC78.

Recommended Operating Conditions

Parameter	Value	Unit
Supply Voltage	3~40	V
Maximum Output Current	300	mA
Operating Ambient Temperature	-40 ~ +85	°C

Electrical Characteristics

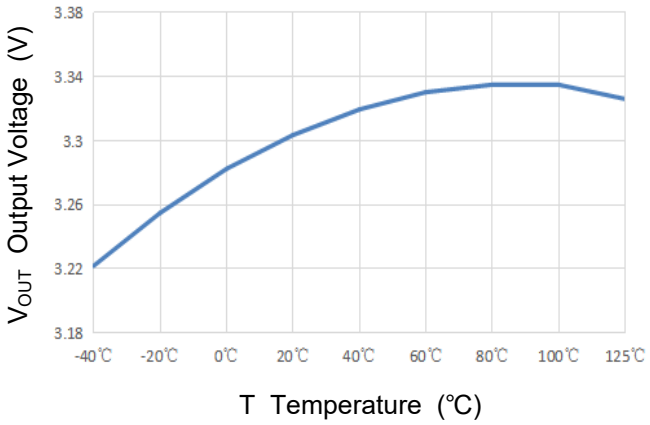
(V_{IN}=V_{OUT}+2V, I_{OUT}=10mA, C_{IN}=1μF, C_{OUT}=1μF, T_A=25℃ , unless otherwise noted.)

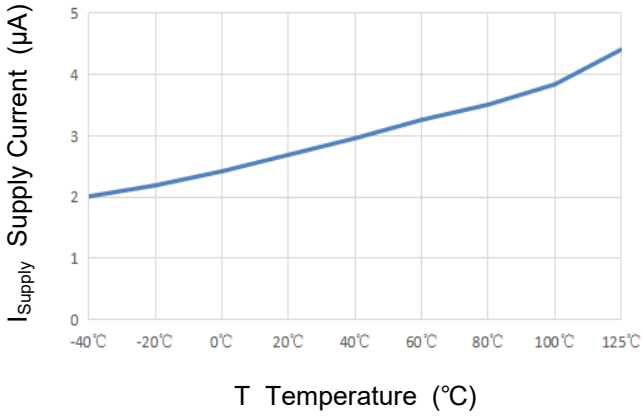
Parameter		Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage		V_{IN}			3	--	40	V
Output Voltage Accuracy		ΔV_{OUT}	T_A=25°C		-1.5	--	+1.5	%
			-40°C ≤ T_A ≤ 85°C		-2	--	+2	%
Quiescent Current		I_Q	I_{OUT}=0mA		--	2.8	6.5	μA
Shutdown Current		I_{Shut}	V_{EN} = 0V, T_A = 25°C		--	0.6	--	μA
Dropout Voltage Note		V_{DROP}	V_{OUT}=1.8V	I_{OUT}=300mA	--	950	1450	mV
			V_{OUT}=3.0V		--	1000	1500	
			V_{OUT}=5.0V		--	1050	1550	
			V_{OUT}=12.0V		--	1100	1600	
Line Regulation		ΔV_{LINE}	V_{IN}=V_{OUT}+1 to 40V, I_{OUT}=10mA		--	20	60	mV
Load Regulation		ΔV_{LOAD}	1mA≤I_{OUT}≤300mA,V_{IN}=V_{OUT}+2V		--	100	150	mV
Current Limit		I_{LIMIT}	V_{IN}=V_{OUT}+2V		--	450	--	mA
EN Pin Current		I_{EN}	V_{EN}=0~40V		--	1	--	μA
Output Noise Voltage		e_N	V_{IN} = V_{OUT}+2V, I_{OUT} = 1mA, f = 10Hz to 100KHz, V_{OUT} =3V,C_{OUT} = 1μF		--	32*V_{OUT}	--	μV_{RMS}
EN Input Threshold	Logic Low	V_{IL}	EN Input Voltage “L”		--	--	0.4	V
	Logic High	V_{IH}	EN Input Voltage “H”		1.4	--	--	V
Power Supply Rejection Ratio		PSRR	V_{IN}=V_{OUT}+2V, I_{OUT}=20mA f=1KHz		--	50	--	dB
Thermal Shutdown Temperature		T_{SHDN}	Shutdown, Temp increasing		--	165	--	°C
Thermal Shutdown Hysteresis		T_{SHDN}	Reset, Temp decreasing		--	25	--	°C

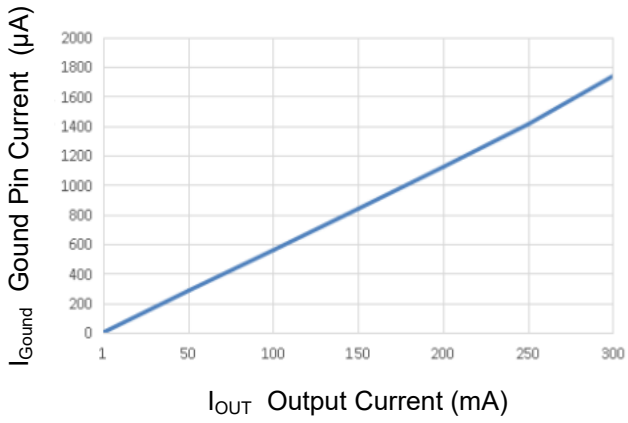
Note: V_{DROP} FT test method: test the V_{OUT} voltage at V_{OUT}+$V_{DROP(MAX)}$ with 300mA output current.

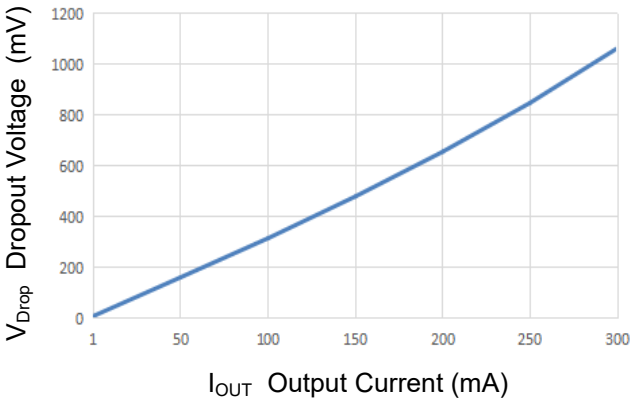
Typical Electrical Curves

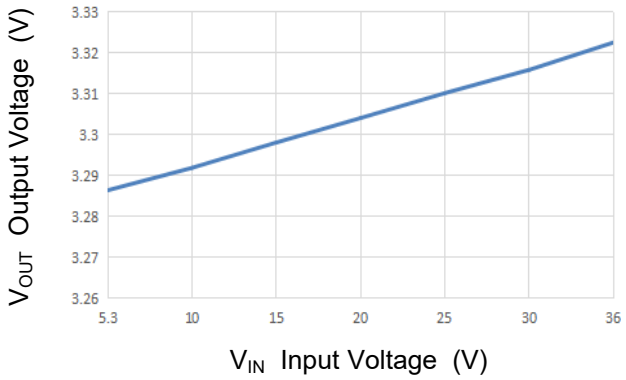
(V_{IN}=V_{OUT}+2V, I_{OUT}=10mA, C_{IN}=1μF, C_{OUT}=1μF, T_A=25℃ , unless otherwise noted.)

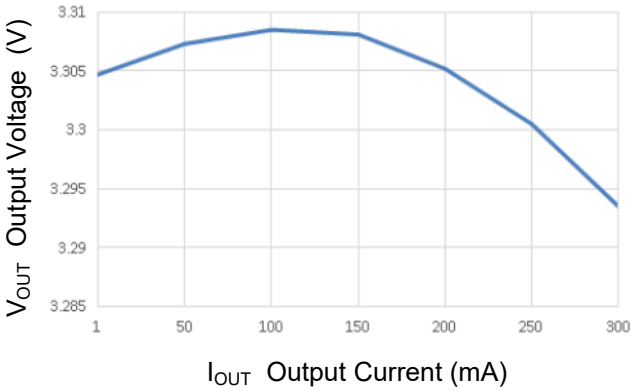


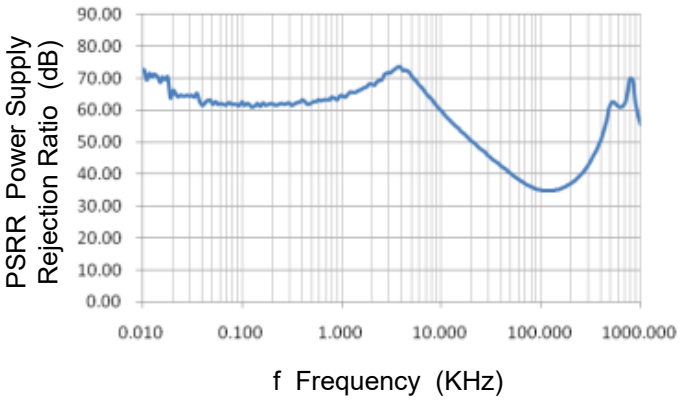


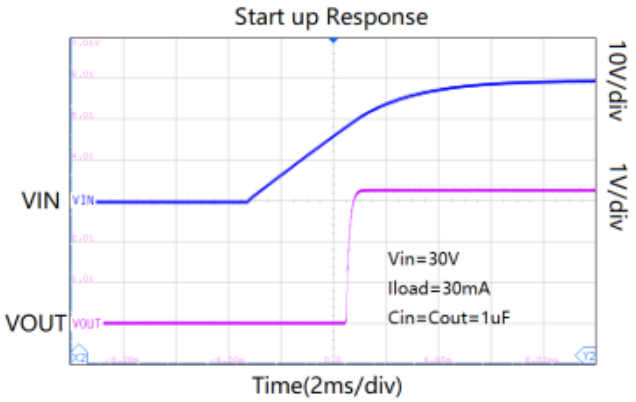


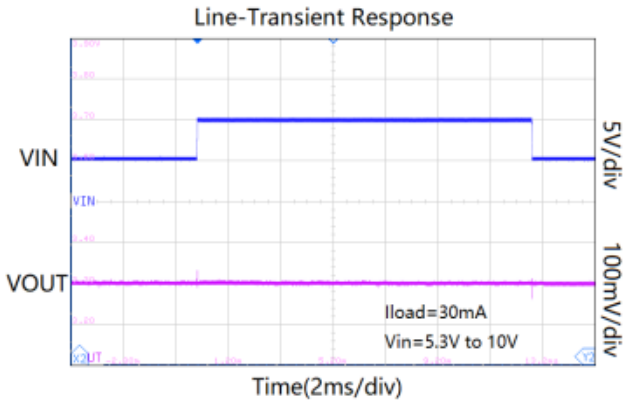


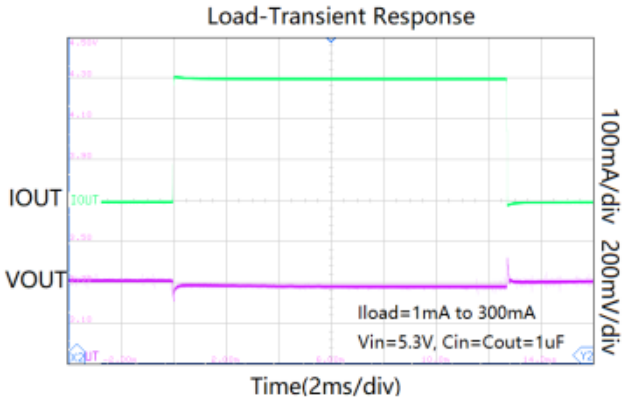





PSRR Power Supply Rejection Ratio (dB)
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
0.010
0.100
1.000
10.000
100.000
1000.000
f Frequency (KHz)


Start up Response
VIN
VOUT
Vin=30V
Iload=30mA
Cin=Cout=1uF
10V/div
1V/div
Time(2ms/div)


Line-Transient Response
VIN
VOUT
Iload=30mA
Vin=5.3V to 10V
5V/div
100mV/div
Time(2ms/div)


Load-Transient Response
IOUT
VOUT
Iload=1mA to 300mA
Vin=5.3V, Cin=Cout=1uF
100mA/div
200mV/div
Time(2ms/div)

Functional Description

Input Capacitor

A 1μF~10uF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Enable

The PJ53 Series delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The PJ53 Series uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155℃.Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $R_{\theta JA}$.

The power dissipation definition in device is:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

Current-Limit Protection

The PJ53 Series provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

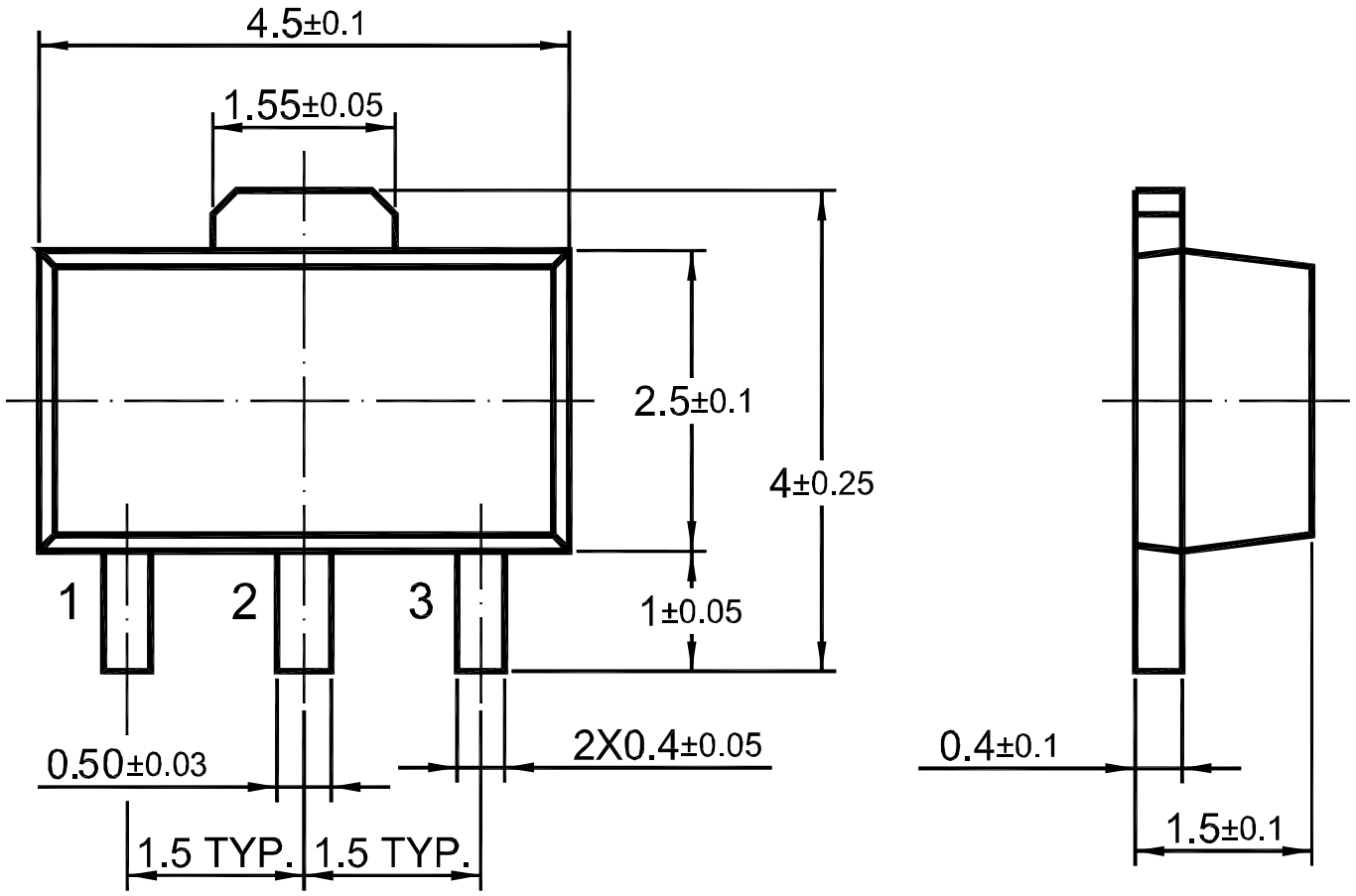
Layout Guidelines

1. Place input and output capacitors as close to the device as possible.
2. Use copper planes for device connections in order to optimize thermal performance.
3. Place thermal vias around the device to distribute heat.

Package Outline

SOT-89

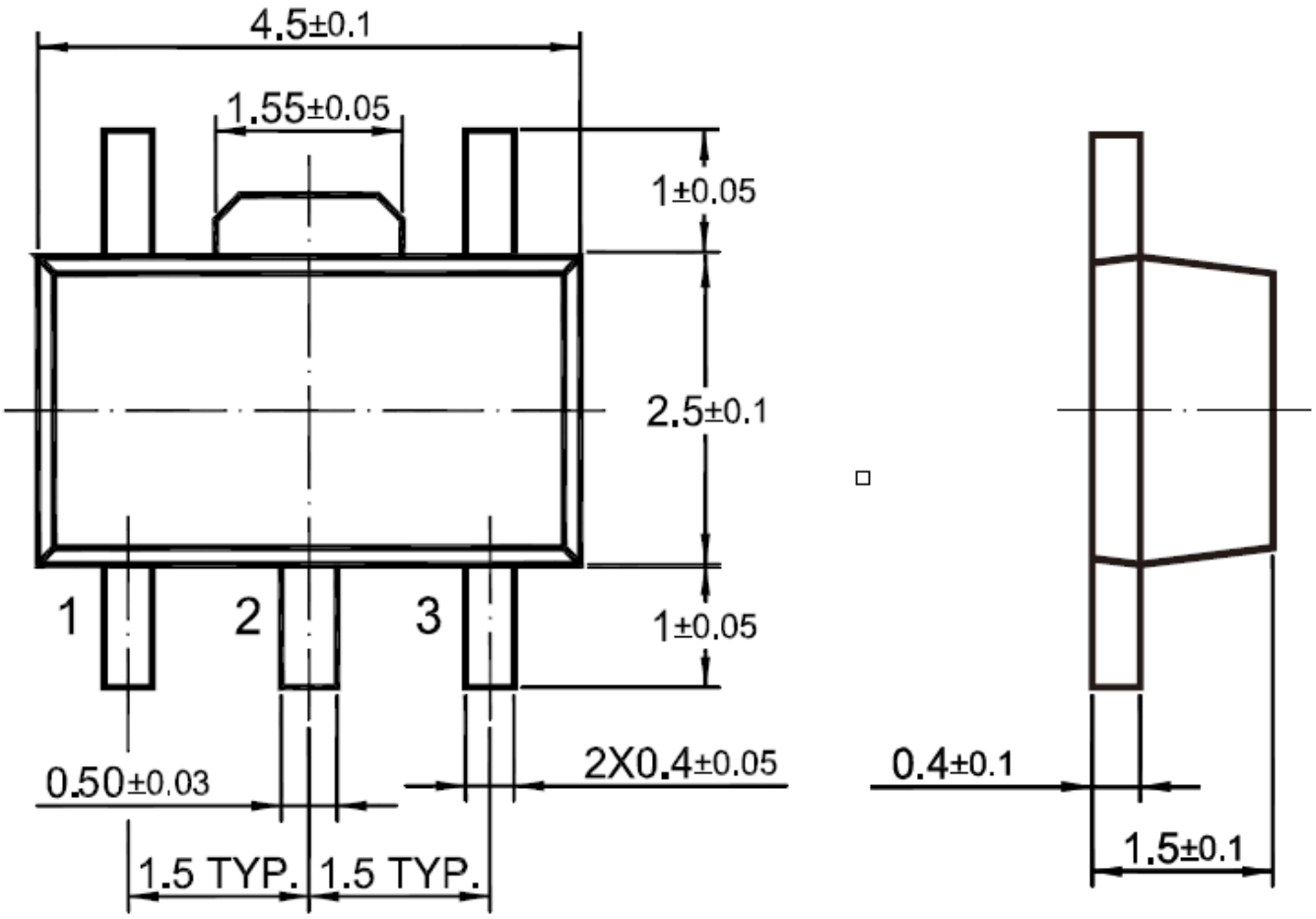
Dimensions in mm



Package Outline

SOT-89-5

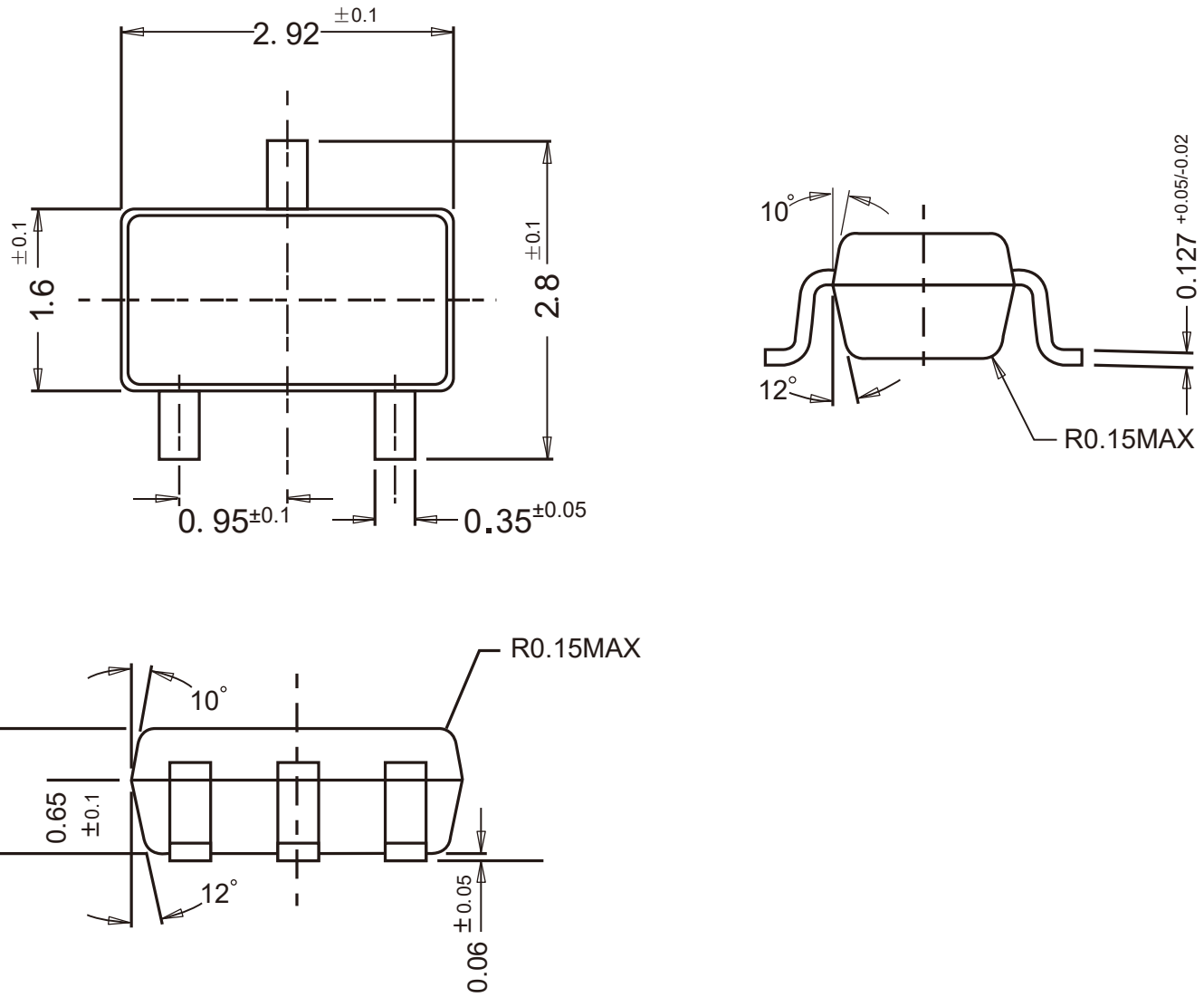
Dimensions in mm



Package Outline

SOT-23-3

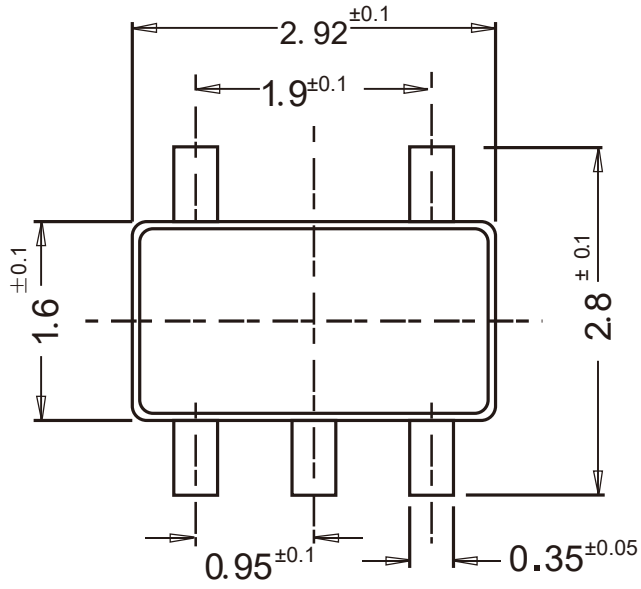
Dimensions in mm

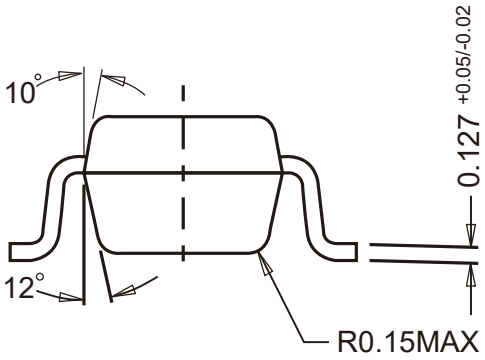


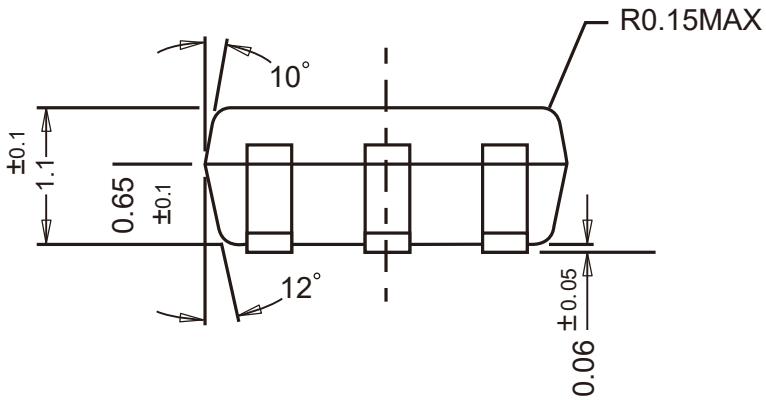
Package Outline

SOT-23-5

Dimensions in mm

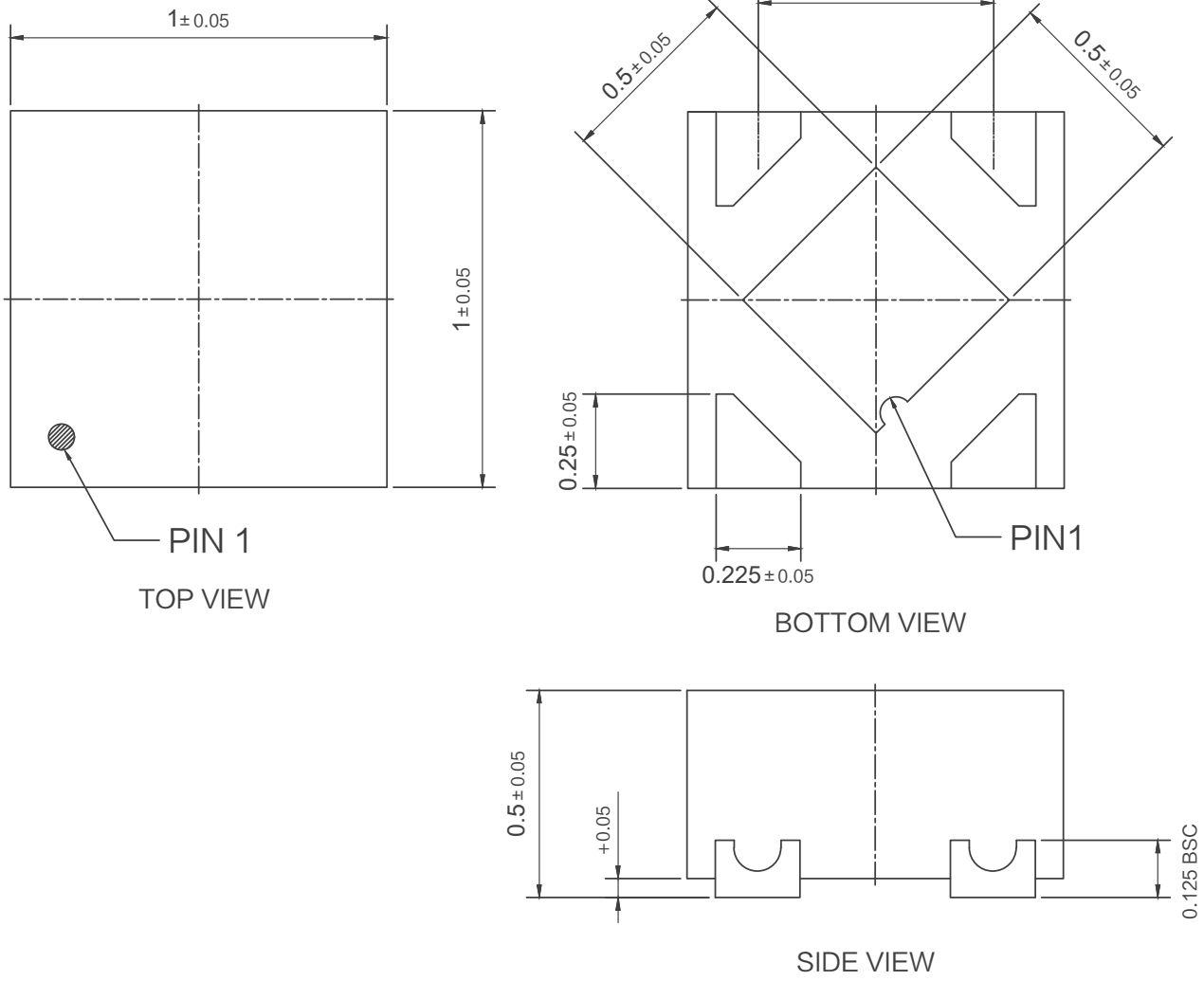






Package Outline

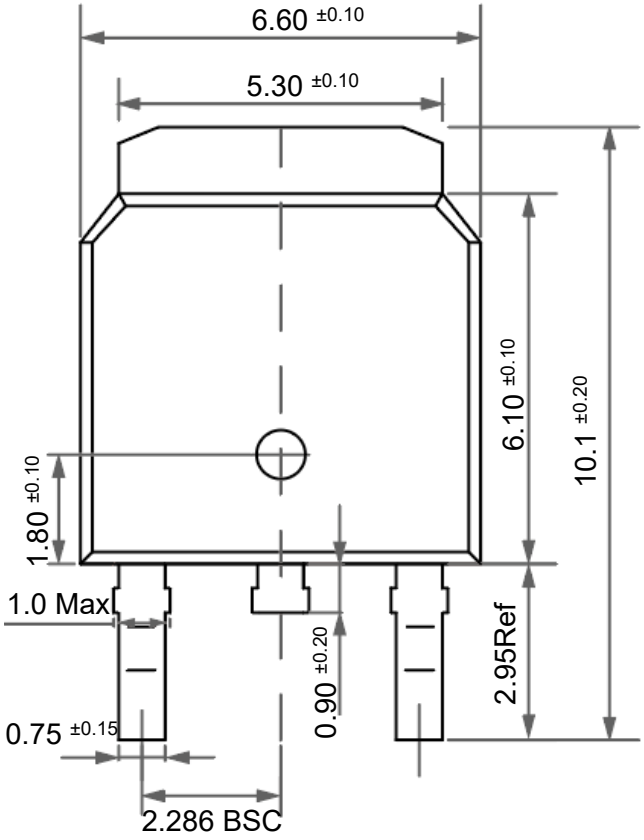
DFN1x1-4L
Dimensions in mm



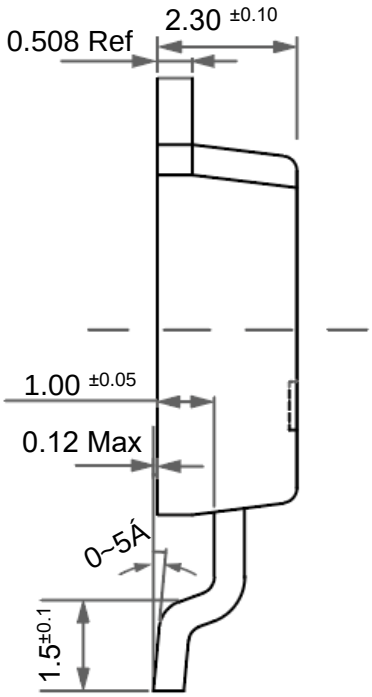
Package Outline

TO-252

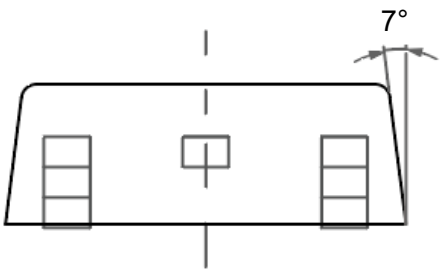
Dimensions in mm



Front View



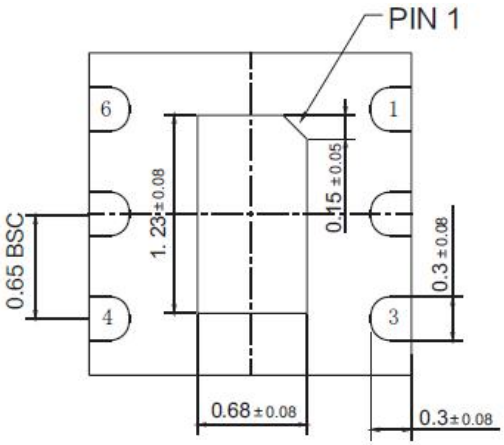
Side View



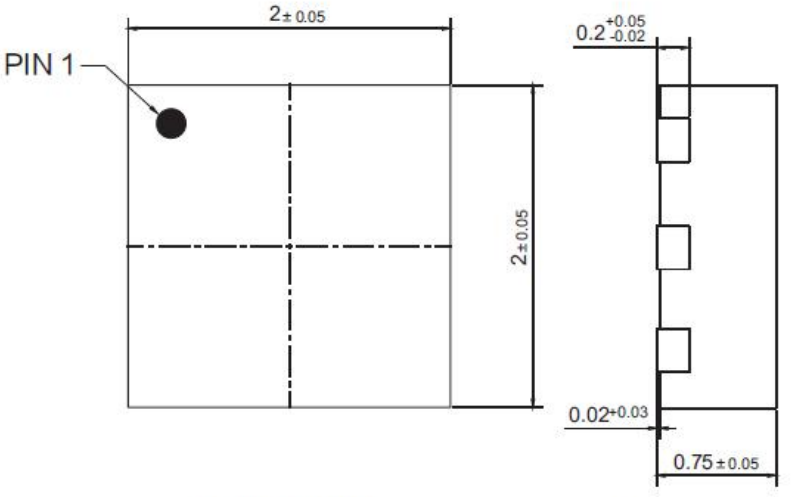
Bottom View

Package Outline

DFN2x2C-6L
Dimensions in mm



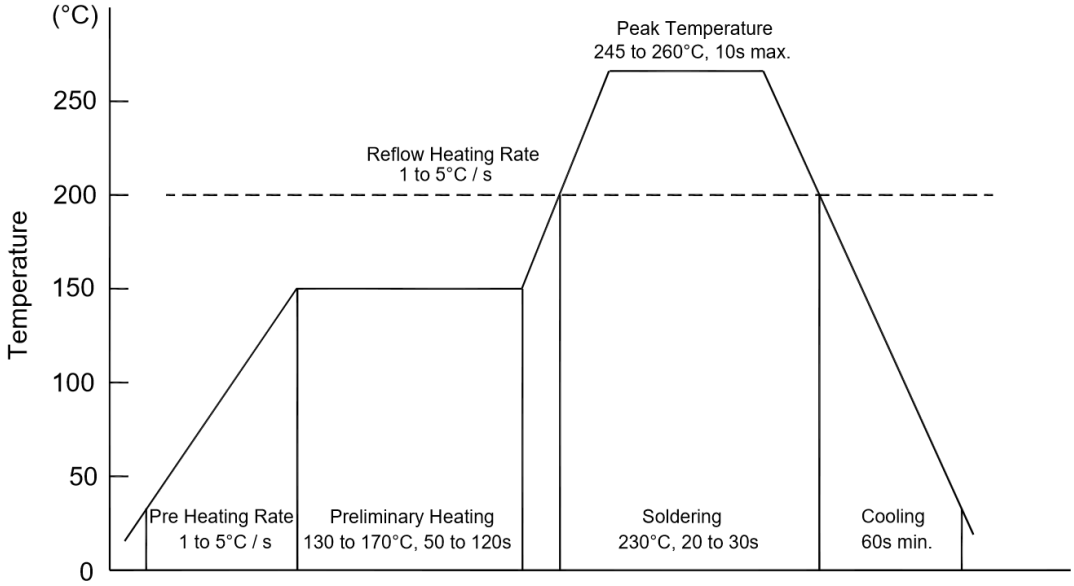
BOTTOM VIEW



TOP VIEW SIDE VIEW

Conditions of Soldering and Storage

◆ Recommended condition of reflow soldering



Recommended peak temperature is over 245°C. If peak temperature is below 245°C, you may adjust the following parameters:

- Time length of peak temperature (longer)
- Time length of soldering (longer)
- Thickness of solder paste (thicker)

◆ Conditions of hand soldering

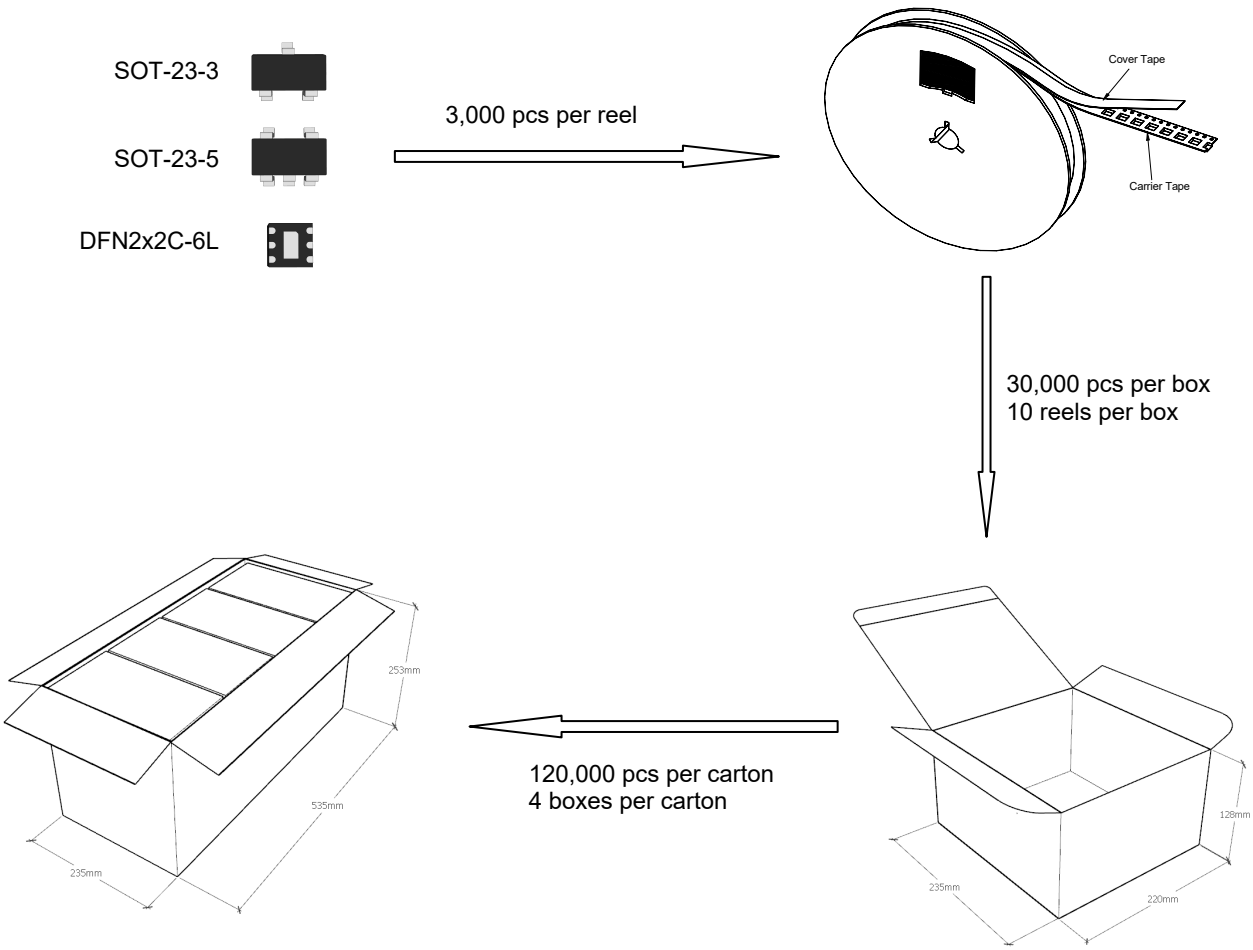
- Temperature: 300°C
- Time: 3s max.
- Times: one time

◆ Storage conditions

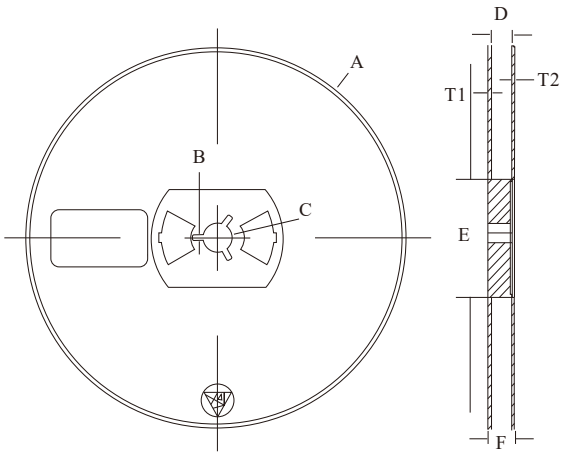
- **Temperature**
  5 to 40°C
- **Humidity**
  30 to 80% RH
- **Recommended period**
  One year after manufacturing

Package Specifications (SOT-23-3/SOT-23-5/DFN2x2C-6L)

- The method of packaging



◆ **reel data**

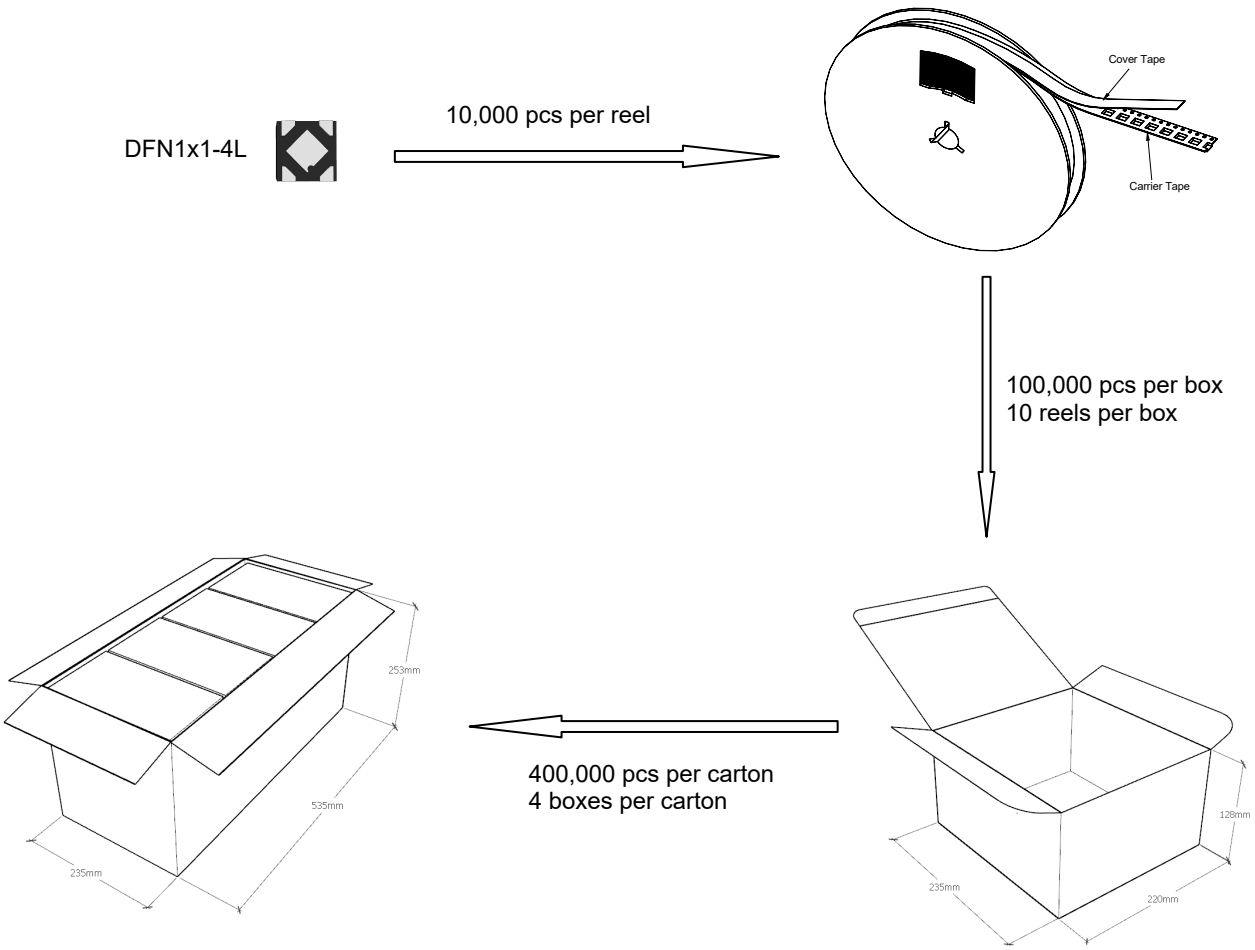


Reel (7")

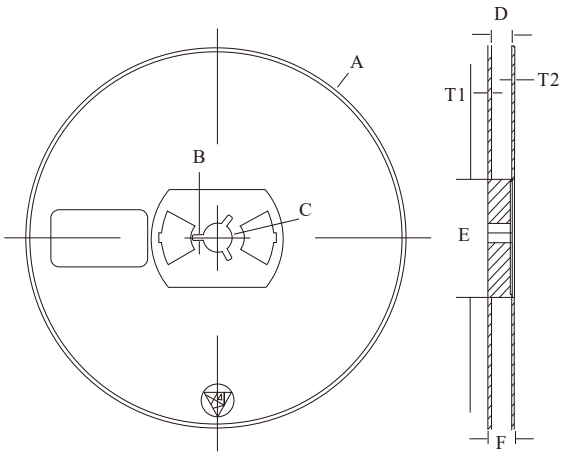
Symbol	Value (unit: mm)
A	Ø 177.8±1
B	2.7±0.2
C	Ø 13.5±0.2
E	Ø 54.5±0.2
F	12.3±0.3
D	9.6+2/-0.3
T1	1.0±0.2
T2	1.2±0.2

Package Specifications (DFN1x1-4L)

- The method of packaging



◆ Embossed reel data

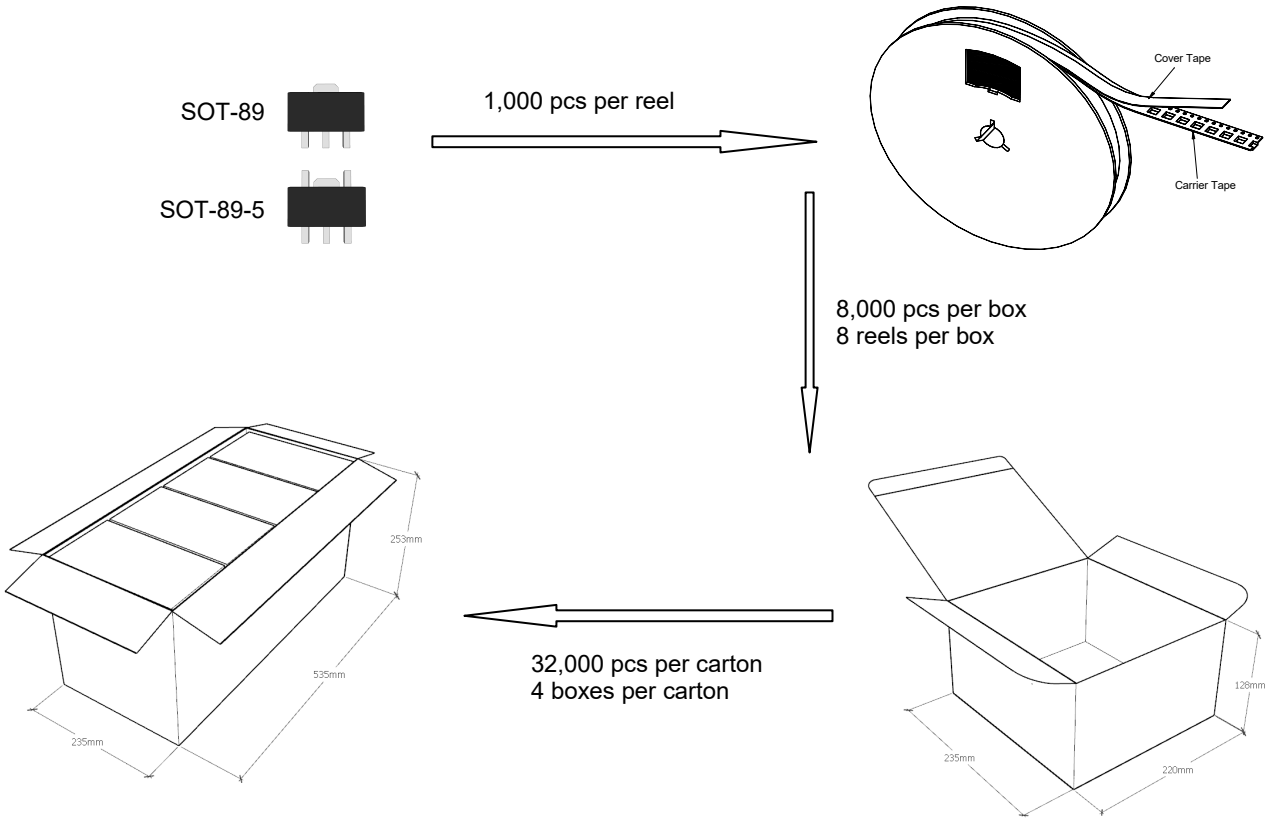


Reel (7")

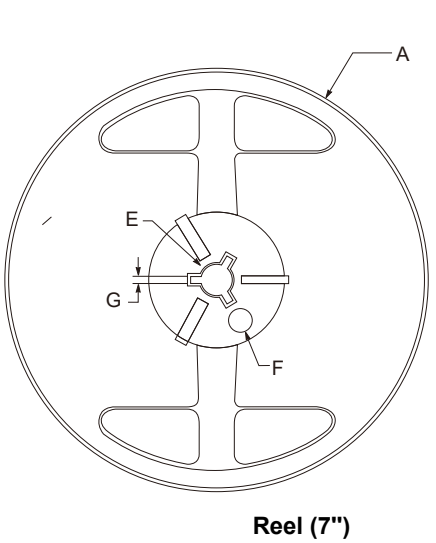
Symbol	Value (unit: mm)
A	Ø 177.8±1
B	2.7±0.2
C	Ø 13.5±0.2
E	Ø 54.5±0.2
F	12.3±0.3
D	9.6+2/-0.3
T1	1.0±0.2
T2	1.2±0.2

Package Specifications (SOT-89/SOT-89-5)

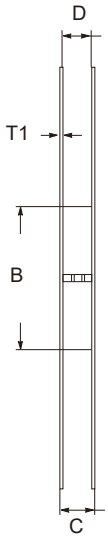
- The method of packaging (1,000PCS/Reel&7inches)



◆ **reel data**



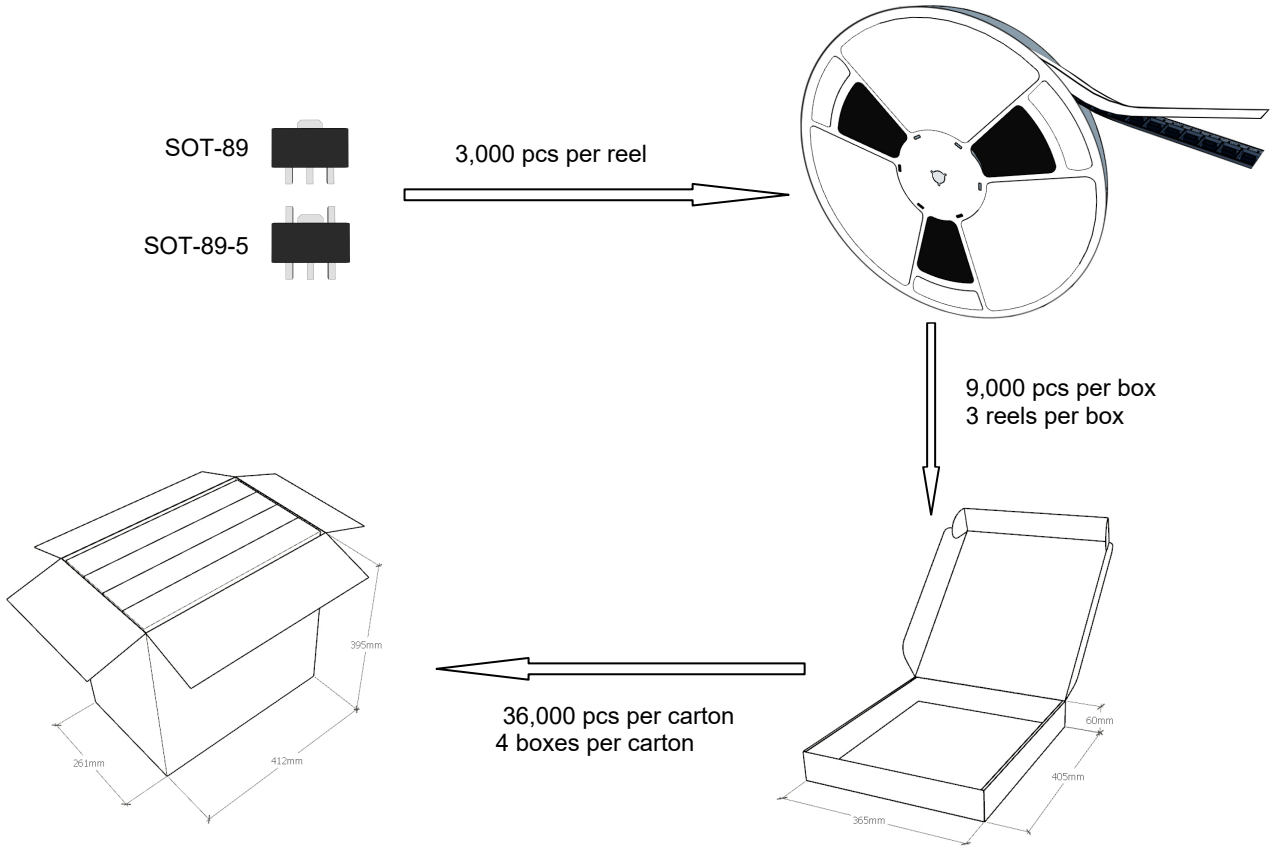
Reel (7")



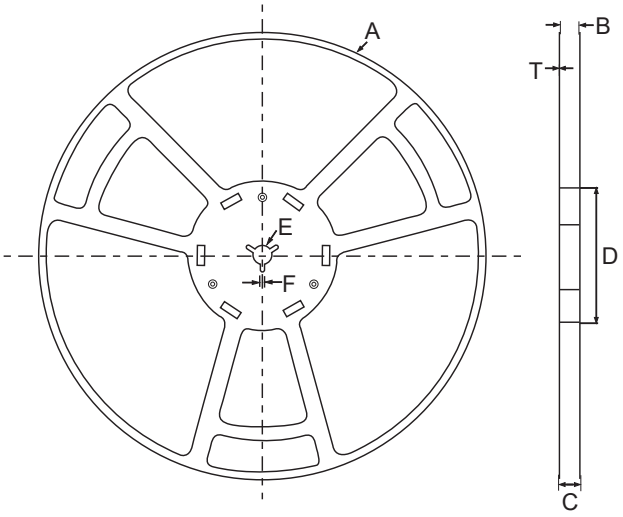
symbol	Value(unit:mm)
A	Φ179±1
B	60.5±0.2
C	15.3±0.3
D	12.5~13.7
E	Φ13.5±0.2
F	Φ10.0±0.2
G	2.7±0.2
T1	1.0±0.2

Package Specifications (SOT-89/SOT-89-5)

- The method of packaging (3,000PCS/Reel&13inches)



◆ **reel data**

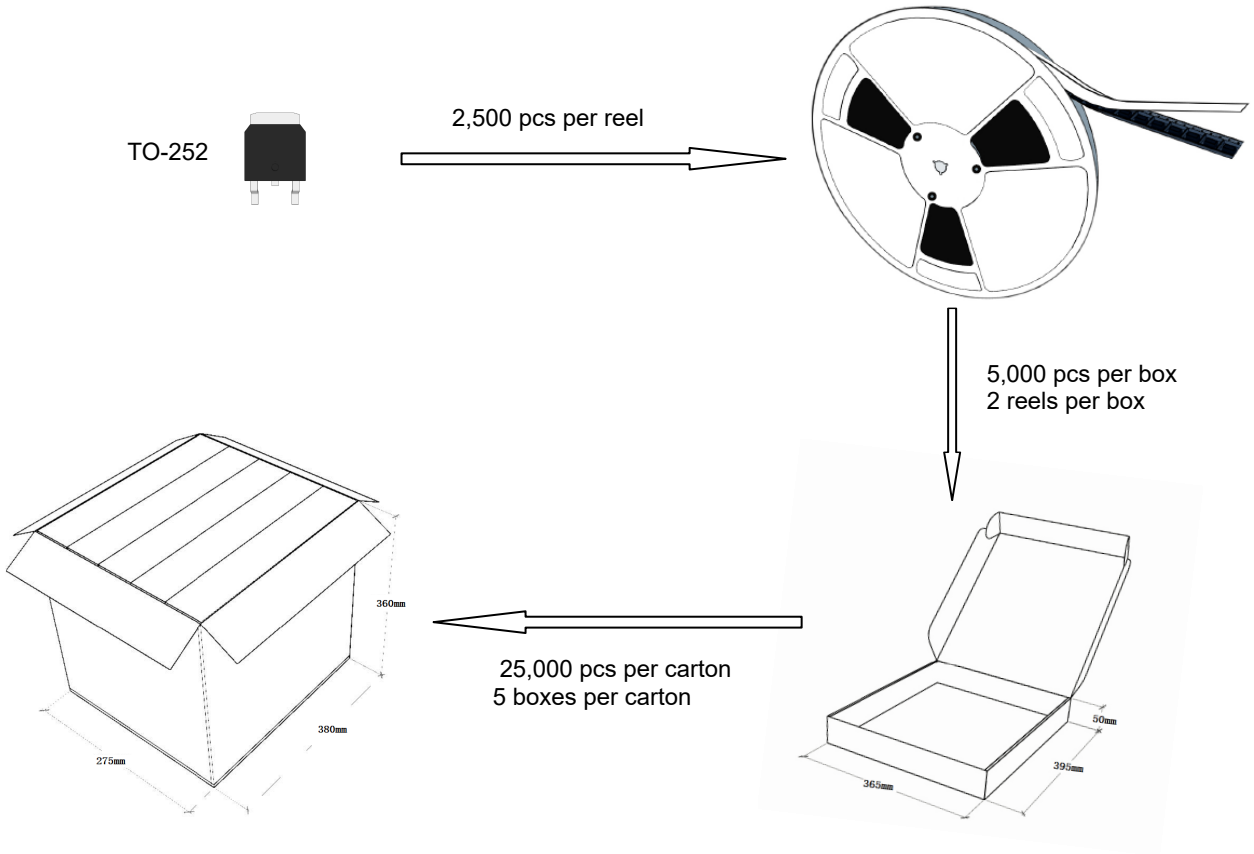


Reel (13")

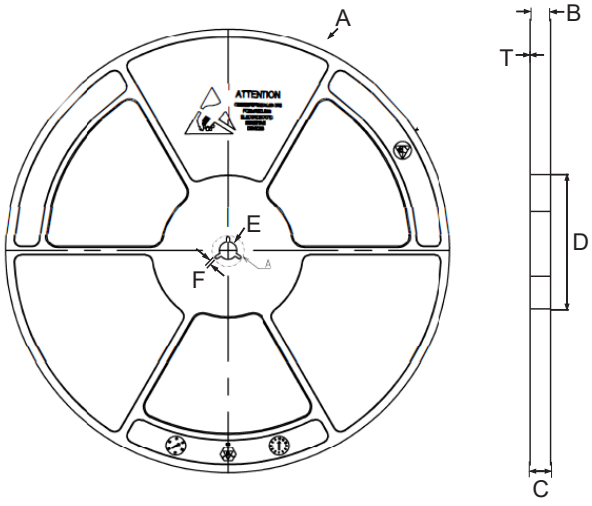
symbol	Value(unit:mm)
A	ϕ330±1
B	12.7±0.5
C	16.5±0.3
D	ϕ99.5±0.5
E	ϕ13.6±0.3
F	2.8±0.3
T	1.9±0.2

Package Specifications (TO-252)

- The method of packaging



- **reel data**

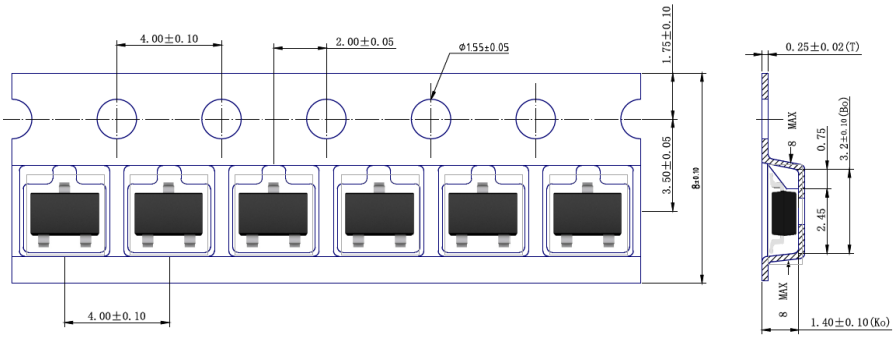


Reel (13")

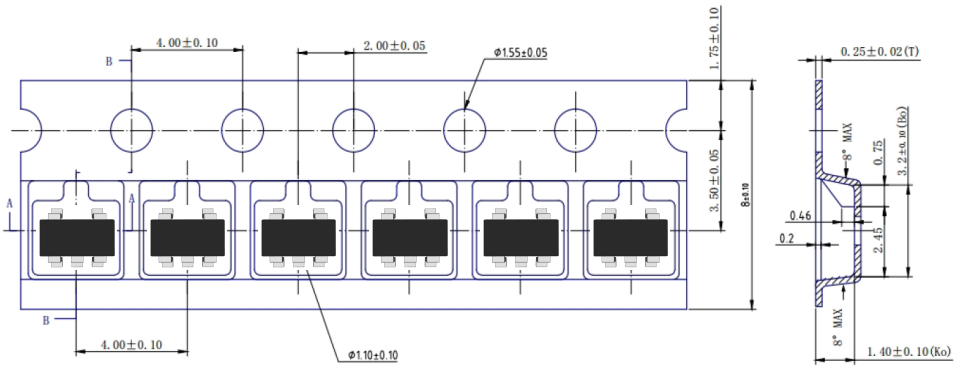
Symbol	Value(unit:mm)
A	Φ330.2±1
B	17±0.5
C	21.2±2
D	Φ100±0.5
E	Φ13.4±0.2
F	2.3±0.2
T	2.1±0.2

◆ Embossed tape data

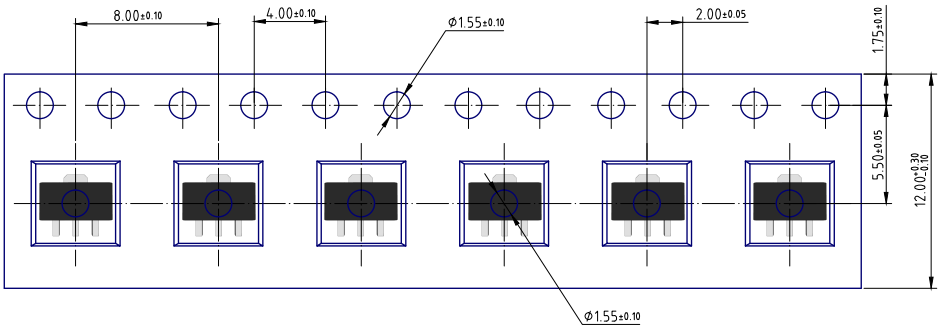
SOT-23-3



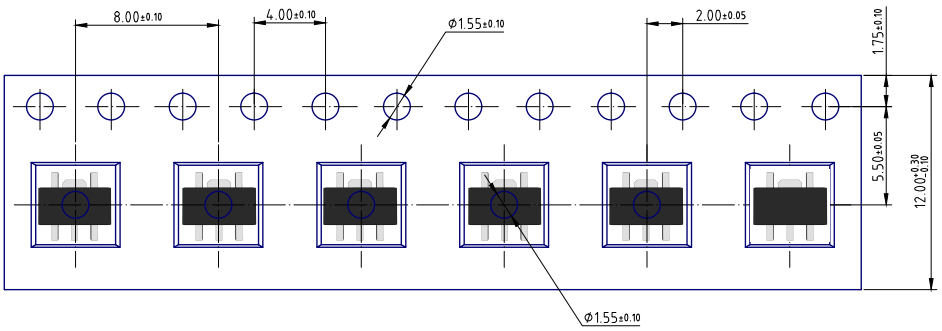
SOT-23-5



SOT-89

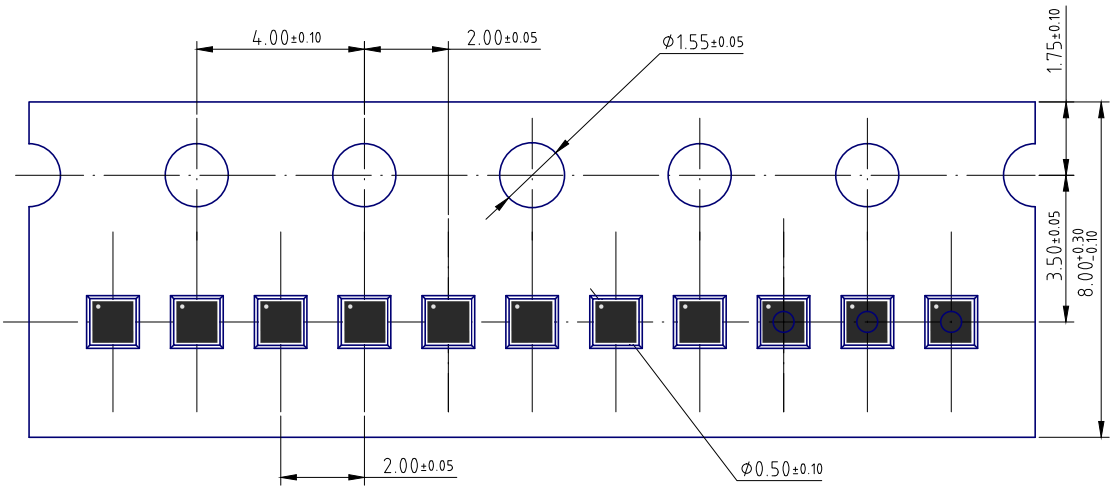


SOT-89-5

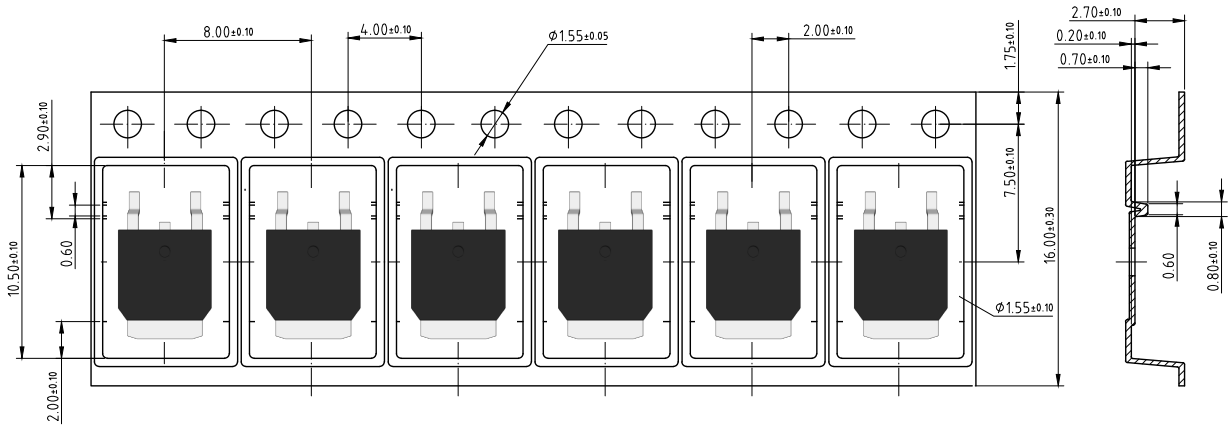


◆ Embossed tape data

DFN1x1-4L



TO-252



DFN2x2C-6L